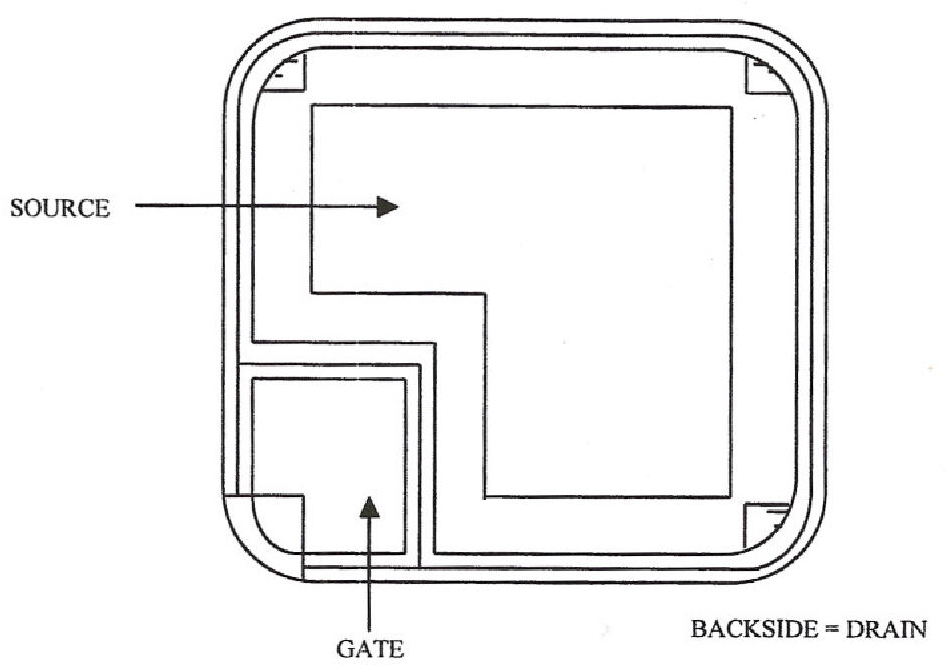
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**Top Material: Al**

**Backside Material: Ti/Ni/Ag/Sn**

**Bond Pad Size:**

**Backside Potential: Drain**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .020” X .020” DATE: 9/23/21**

**MFG: FAIRCHILD SEMI THICKNESS .008” P/N: BSS84**

**DG 10.1.2**

#### Rev B, 7/19/02